Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.041”**

**.041”**

**EMITTER**

**.0085”**

**BASE Ø**

**.006”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size:**

**Backside Potential: COLLECTOR**

**Mask Ref: G10**

**APPROVED BY: DK DIE SIZE .041” X .041” DATE: 10/19/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .008” P/N: ZTX653**

**DG 10.1.2**

#### Rev B, 7/19/02